We claim:

1. An impedance matched write circuit, comprising:

an interconnect for connecting to a write head;

at least one resistor between a control voltage and said interconnect for impedance matching to said interconnect; and

a transistor connected across said at least one resistor to shunt at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode.

2. The impedance matched write circuit of claim 1, wherein said transistor comprises a PMOS transistor.

3. The impedance matched write circuit of claim 1, wherein said transistor comprises a combination of PMOS and NMOS transistors.

4. The impedance matched write circuit of claim 1, wherein drain and source connections of said transistor are connected to each side of said at least one resistor.

5. The impedance matched write circuit of claim 1, wherein a gate voltage of said transistor is controlled by a gate voltage source such that said transistor is turned on in an overshoot mode.

6. The impedance matched write circuit of claim 1, wherein a gate voltage of said transistor is controlled by a gate voltage source such that said transistor is turned off during a steady state mode.

7. The impedance matched write circuit of claim 5, wherein said gate voltage source comprises a resistor between a source and a gate of said transistor and a current source from said gate to a negative supply voltage.

8. The impedance matched write circuit of claim 7, wherein said current source is turned on during an overshoot mode.

9. The impedance matched write circuit of claim 7, wherein said current source is turned off during a steady state mode.

10. The impedance matched write circuit of claim 1, further comprising:

a first current source at a first side of said interconnect when a voltage at the first side of the interconnect is low; and

a second current source at a second side opposite the first side of the interconnect when a voltage at the second side of the interconnect is low.

11. An impedance matched write circuit, comprising:

an interconnect for connecting to a write head;

at least one resistor between a control voltage and said interconnect for impedance matching to said interconnect; and

means for shunting at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode.

12. The impedance matched write circuit of claim 11, wherein said means for shunting current comprises a transistor.

13. The impedance matched write circuit of claim 12, wherein said transistor comprises a PMOS transistor.

14. The impedance matched write circuit of claim 12, wherein said transistor comprises a combination of PMOS and NMOS transistors.

15. The impedance matched write circuit of claim 12, wherein drain and source connections of said transistor are connected to each side of said at least one resistor.

16. The impedance matched write circuit of claim 12, wherein a gate voltage of said transistor is controlled by a gate voltage source such that said transistor is turned on in an overshoot mode.

17. A method for impedance matching in a write circuit, comprising the steps of:

connecting to a write head using an interconnect;

providing at least one resistor between a control voltage and said interconnect for impedance matching to said interconnect; and

shunting at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode.

18. The method of claim 17, wherein said shunting current step is performed by a transistor.

19. The method of claim 18, wherein said transistor comprises a PMOS transistor.

20. The method of claim 18, further comprising the step of connecting drain and source connections of said transistor to each side of said at least one resistor.

21. The method of claim 18, further comprising the step of controlling a gate voltage of said transistor by a gate voltage source such that said transistor is turned on in an overshoot mode.